Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing Of Claims:

1. (Previously presented) A coding device comprising:

a coding circuit configured to generate a coded output from a digital input;

an interleaving circuit configured to generate a plurality of interleaved words from said coded output; and

a rate matching circuit for adjusting the number of bits in a data block comprising said plurality of interleaved words, the coded output having a greater number of bits than the digital input, the rate matching circuit having means for adjusting the number of bits in the data block using a rate matching pattern to provide data bits for transmission during respective frames of a transmission channel, and means for selecting the rate matching pattern depending on an associated bit deletion or repetition pattern that is selected to ensure that deleted or repeated bits of the data block are not required to enable all bits from the digital input to be reconstructed.

2. (Canceled)

3. (Previously presented) A coding device as claimed in claim 1, wherein the rate matching pattern for each interleaved word within the data block is offset with respect to the rate matching pattern of an adjacent interleaved word or words within the block.

4. (Previously presented) A coding device as claimed in claim 1, wherein the rate matching pattern is selected as a function of an interleaving depth of the interleaving circuit.

5. (Cancelled)

6. (Previously presented) A decoding device for decoding a signal coded by a coding device having a rate matching circuit for adjusting the number of bits in a data block, the data bock comprising a plurality of interleaved words generated by the action of an interleaving circuit on a coded output generated by the action of a coding circuit on a digital input, the coded output having a greater number of bits than the digital input, the rate matching circuit having means for adjusting the number of bits in the data block using a rate matching pattern to provide data bits for transmission during respective frames of a transmission channel, and means for selecting the rate matching pattern depending on an associated bit deletion or repetition pattern that is selected to ensure that deleted or repeated bits of the data block are not required to enable all bits from the digital input to be reconstructed, said decoding device comprising a data reconstruction circuit for reconstructing the interleaved words, a de-interleaving circuit and a channel decoder.

Claim 7-10 (Cancelled)

11. (Currently amended) The coding device of claim 1, wherein the rate matching pattern forms a matrix including change bits that indicate a change of corresponding

bits of a matrix of said interleaved words within said data block, wherein each row of said matrix formed by the rate matching pattern includes a maximum of one of said change bits.

12. (Previously presented) The coding device of claim 1, wherein said coding circuit has one of: (a) a fixed code rate and (b) a predetermined number of rates for a variable data source.

13. (Previously presented) The coding device of claim 1, wherein said interleaving circuit is not adaptive.

14. (Previously presented) The coding device of claim 1, wherein said interleaving circuit has a constant input bit rate.

15. (Previously presented) The coding device of claim 1, wherein said coding circuit has one of: (a) a fixed code rate and (b) a predetermined number of rates for a variable data source, and wherein said interleaving circuit is not adaptive.

16. (Previously presented) The coding device of claim 1, wherein said rate matching circuit alters a coding rate of said coding circuit according to the bit deletion or repetition pattern.

17. (Previously presented) A decoding device for decoding a coded digital signal comprising a received data block including interleaved words, said received data block having

been processed by a rate matching circuit using a rate matching pattern to adjust a number of bits in said received data block, the decoding device comprising:

a data reconstruction circuit having means for adjusting the number of bits in said received data block to reverse action of said rate matching circuit, thereby reconstructing said interleaved words;

a de-interleaving circuit having means for generating each of said interleaved words; and

a channel decoder which receives said interleaved words provided by said de-interleaving circuit;

wherein said rate matching pattern is selected as a function of a bit deletion or repetition pattern having been selected to ensure that deleted or repeated bits of the received data block are not required to enable all bits from the digital input to be reconstructed.

18. (Previously presented) The decoding device of claim 17, wherein said rate matching pattern includes change bits for deleting or repeating bits of said data block and the change bits are offset with respect to each other along adjacent rows or columns of a matrix of said rate matching pattern.

19. (Previously presented) A method of decoding a coded digital signal comprising a received data block including interleaved words, said received data block having been processed by a rate matching circuit using a rate matching pattern to adjust a number of bits in said received data block, the method comprising:

adjusting the number of bits in said received data block to reverse action of said rate matching circuit, thereby reconstructing said interleaved words;

generating each of said interleaved words; and

receiving said interleaved words;

wherein said rate matching pattern is selected as a function of a bit deletion or repetition pattern having been selected to ensure that deleted or repeated bits of the received data block are not required to enable all bits from the digital input to be reconstructed.

20. (Previously presented) The method of claim 19, wherein said rate matching pattern includes change bits for deleting or repeating bits of said data block and said change bits are offset with respect to each other.

21. (Previously presented) The method of claim 19, wherein said rate matching pattern includes change bits for deleting or repeating bits of said data block and said change bits are offset with respect to each other along adjacent columns of a matrix of said rate matching pattern.

22. (Previously presented) The method of claim 19, wherein said rate matching pattern includes change bits for deleting or repeating bits of said data block and said change bits are offset with respect to each other along adjacent rows of a matrix of said rate matching pattern.

23. (Previously presented) The method of claim 19, wherein said rate matching pattern includes change bits for deleting or repeating bits of said data block and said change bits

are offset with respect to each other along adjacent rows and columns of said rate matching pattern.

24. (Previously presented) The method of claim 19, wherein said received data block is formed by filling a matrix row by row with row bits of said coded output and outputting column bits of said matrix column by column to form said interleaved words.

25. (Previously presented) A method of coding a digital signal comprising:

generating a coded output from a digital input;

generating a plurality of interleaved words from said coded output; and

adjusting the number of bits in a data block comprising said plurality of interleaved words using a rate matching pattern to provide data bits for transmission during respective frames of a transmission channel; and

selecting the rate matching pattern depending on a bit deletion or repetition pattern is selected to ensure that deleted or repeated bits of the data block are not required to enable all bits from the digital input to be reconstructed.

26. (Previously presented) The method of claim 25, wherein said rate matching pattern includes change bits for deleting or repeating bits of said data block and said change bits are offset with respect to each other.

27. (Previously presented) The method of claim 25, wherein said rate matching pattern includes change bits for deleting or repeating bits of said data block and said change bits

are offset with respect to each other along adjacent columns of a matrix of said rate matching pattern.

28. (Previously presented) The method of claim 25, wherein said rate matching pattern includes change bits for deleting or repeating bits of said data block and said change bits are offset with respect to each other along adjacent rows of a matrix of said rate matching pattern.

29. (Previously presented) The method of claim 25, wherein said rate matching pattern includes change bits for deleting or repeating bits of said data block and said change bits are offset with respect to each other along adjacent rows and columns of said rate matching pattern.

30. (Previously presented) The method of claim 25, wherein data block is formed by filling a matrix row by row with row bits of said coded output and outputting column bits of said matrix column by column to form said interleaved words.